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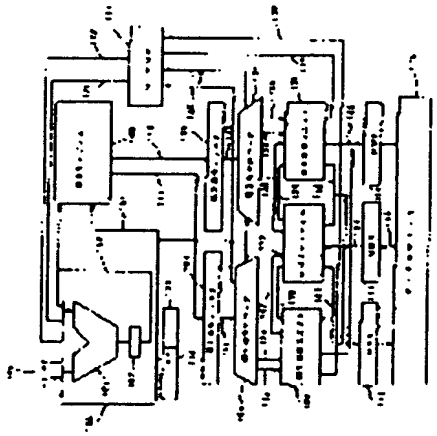
(54) DEVICE AND METHOD FOR PARALLEL PROCESSING

(57)Abstract:
PURPOSE: To improve throughput by providing a means to selectively execute plural instruction parallel processing and sequential processing.
CONSTITUTION: Two instructions are read out from an instruction cache 100 when the value of a processing state flag PE116 in a processor status register 103 is turned on, and they are set at a first instruction register 104 and a second instruction register 105, and are processed in parallel with a first arithmetic unit 108 and a second arithmetic unit 109. Meanwhile, when the value of the flag PE116 is turned off, one instruction is read out from the instruction cache 100 to the first instruction register 104, and is processed with the first arithmetic unit 108, and also, the second arithmetic unit 109 is stopped, then, the sequential processing with the first arithmetic unit 108 is performed. In such a way, fast processing can be executed by using a high-level parallel processing function.



LEGAL STATUS

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